IN THE CLAIMS

1-46. (Canceled)

47. (Currently Amended) ~~The~~ A memory ~~of claim 46~~, comprising:

a memory array;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array; and

wherein the memory array, control circuit and I/O circuit each comprise:

a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer; and

wherein the titanium alloy comprises titanium and zinc.

48-60. (Canceled)

61. (Currently Amended) ~~The memory device of claim 60~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy

comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer,

wherein the titanium alloy comprises titanium and zinc.

62-64. (Canceled)

65. (Currently Amended) ~~The memory device of claim 64~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer,

wherein the titanium alloy includes titanium and zinc.

66-68. (Canceled)

69. (Currently Amended) ~~The memory device of claim 68~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphosilicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the borophosphosilicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer,

wherein the titanium alloy includes titanium and zinc.

70-72. (Canceled)

73. (Currently Amended) ~~The memory device of claim 72~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer,

wherein the titanium alloy includes titanium and zinc.

74-77. (Canceled)

78. (Currently Amended) ~~The memory device of claim 77~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer,

wherein the titanium alloy includes titanium and zinc.

79-81. (Canceled)

82. (Currently Amended) ~~The memory device of claim 81~~ A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphosilicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphosilicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer, wherein the titanium alloy includes titanium and zinc.

83. (Previously Presented)A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises

a layer of a titanium alloy formed by chemical vapor deposition at a temperature range of 300 to 550 degrees Centigrade at a gas pressure range of 0.1 torr to 10 torr, and overlying walls of a contact hole with a step coverage of more than 90%; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.

84. (Previously Presented)The memory device of claim 83, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony.